

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Won-Sang Song, et al.

Serial No.: not yet assigned Art Unit: not yet assigned

Filed: January 27, 2004 Examiner: not yet assigned

For: APPARATUS FOR TESTING RELIABILITY OF
INTERCONNECTION IN INTEGRATED CIRCUIT

Mail Stop Patent Applications
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant submits herewith PTO Form 1449 listing patents and publications of which he is aware which may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR Section 1.56.

The above-referenced application is a divisional of U.S. Serial No. 10/114,735, filed April 1, 2002, and is now pending.

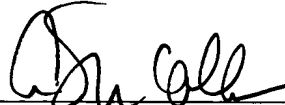
It includes the same disclosure as U.S. patent application Serial No. 10/114,735.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application. 37 CFR Section 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

Customer No. 20575

Respectfully submitted,

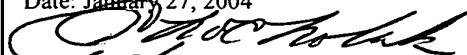
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Date: January 27, 2004


Adrienne Chocholak

PATENT APPLICATION
Docket No. 4591-370

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NTEGRATED CIRCUIT

INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

<u>Exam</u> <u>Init</u>	<u>Ref</u>	<u>Document</u> <u>Number</u>	<u>Issue</u> <u>Date</u>	<u>Name</u>	<u>Class</u>	<u>Sub</u> <u>Class</u>
_____	_____	6,054,721	4/25/2000	Milor		
_____	_____	6,297,644	10/2001	Jarvis, et al.		
_____	_____	5,900,735	5/1999	Yamamoto		
_____	_____	5,514,974	5/1996	Bouldin		

Examiner: _____

Date Considered: _____